Digital Design

(a) Consider the following combinational circuit implementing the parity check on 8 inputs x1,…, x8

(i) What is the total number of tests to detect stuck-at-1 logic fault on input line x1 ?
(ii) What is the total number of tests to detect stuck-at-1 logic fault on input line x8 ?
(iii) Consider the following 'complex' fault model: single stuck-at-1 fault can occur ***either*** on line x1 ***or*** on line x8. What is the total number of tests to detect this 'complex' logic fault ?
(iv) Consider the following 'complex' fault model: single stuck-at-1 fault can occur on **both** lines x1 and x8. What is the total number of tests to detect this 'complex' logic fault ?

Grading: 0.5 pts for each part (i) – (iv).

(b) Consider the ripple counter shown below. Assume that all flip-flops are positive edge-triggered. Show the transition diagram for this counter, and clearly show the transition states. Determine the counting sequence for this ripple counter assuming the initial state 000. Is this counter self-starting?
Note: the counter is self-starting if the states in the counting sequence can be reached from any other state in the transition diagram.

Grading: 2 pts